REMARKS

Claims 1, 3, 5-9, 11, 13 and 14 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest (US 6,226,338), claims 2, 10 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest in view of the newly cited Ngai et al. (US 6,400,635 B1), claims 4 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest in view of Begur et al. (US 5,784,649), and claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest in view of Ngai et al. and in further view of Begur et al. These rejections are respectfully disagreed with, and are traversed below.

It was previously pointed out that at least one patentably distinguishable feature of this invention can be seen by simply comparing Figure 2 of this patent application to Figures 2, 3 and 7 of Earnest. That is, in Figure 2 of this patent application it can be seen that there is a single dual port memory (RAM) 18, whereas in Earnest there is a transmit FIFO 16, a receive FIFO 18, and a corresponding transmit dual port RAM 100 and receive dual port RAM 200. In order to further highlight this important distinction between this invention and Earnest claim 1 was previously amended to recite in part that the programmable buffer circuit includes:

> "a single dual port memory having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;
>
> an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus for selectively storing data in and reading data from said single dual port memory;
>
> an address generator for generating dual port memory addresses for selectively reading data from and writing data to said single dual port memory using said CPU data bus and said channel data bus; and
>
> an allocator and control unit programmable by said CPU for specifying individual ones of buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, and for enabling individual ones of said buffers, said allocator having outputs coupled to said address generator for

> controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said single dual port memory." (emphasis added)

In addition, the independent method claim 9 was previously amended to also recite the use of a single dual port memory, and to state that generating dual port memory addresses is for "selectively reading data from and writing data to said single dual port memory using said CPU data bus and said channel data bus."

It was then argued that claims 1 and 9, as even further clarified by amendment, are clearly not anticipated or rendered unpatentable by the two FIFO, two dual port RAM embodiment disclosed by Earnest. For example, Earnest states in col. 2, line 66, to col. 3, line 6:

> "Core 14 is coupled to DMA controller 20 through transmit FIFO 16 and receive FIFO 18. **Transmit FIFO 16 and receive FIFO 18 each include a single random access memory (RAM) device** for buffering data between core 14 and DMA controller 20. The memory locations within each RAM device are divided into blocks, or "queues", with one queue being associated with a corresponding one of the logical channels" (emphasis added).

Reference can also be made to col. 4, lines 33-36:

> "The data communication circuit shown in FIG. 1 uses **a single memory device for all logical channels in transmit FIFO 16 and a single memory device for all logical channels in receive FIFO 18**" (emphasis added).

Reference can also be had to col. 11, line 56, to col. 12, line 3, where it is stated (in part) that:

> "The data communication circuit of the present invention uses **a single, shared FIFO device for all transmit channels and a single, shared FIFO device for all receive channels**" (emphasis added).

In the most recent office action the Examiner argues that while Earnest discloses multiple dual port memories instead of a single dual port memory, "Making something integral, such as

multiple memories into a single memory, is not a patentable concept", etc.

However, the Applicants are claiming more than just the use of single memory in place of two memories. As was recited above, claim 1 also claims aspects of this invention that relate to the control and use of the single dual port memory, e.g.: "an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus **for selectively storing data in and reading data from said single dual port memory**; an address generator for generating dual port memory addresses for **selectively reading data from and writing data to said single dual port memory** using said CPU data bus and said channel data bus; and **an allocator and control unit programmable by said CPU for specifying individual ones of buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces**, and for enabling individual ones of said buffers, said allocator having outputs coupled to said address generator for controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said single dual port memory" (emphasis added).

Thus, since Earnest intentionally elects to provide separate memory devices for implementing the transmit and receiver buffers, and discusses at length his rationale for doing so (see, for example, col. 4, lines 36-49, and col. 11, line 58, to col. 12, line 3) he thereby teaches away from the single dual port memory embodiments of this invention, as presently claimed.

Further, the claimed "single dual port memory" in accordance with embodiments of this invention is not claimed in isolation, but there are also claimed various aspects of the use and control of the "single dual port memory". Thus, the claimed embodiments of this invention go beyond merely providing an integrally made assembly having two functions, where the prior art shows several parts (functions) that are rigidly secured together as a single unit, as in *In re Larson* that is cited in MPEP 2144.04.V.B.

Clearly Earnest does not have an express disclosure of, or a suggestion to, provide a programmable buffer circuit and method that includes a single dual ported memory device.

In that claims 1 and 9 are not made obvious by Earnest, then claims 2-8 and 10-14 are not anticipated by Earnest, nor or they rendered unpatentable over Earnest alone or in view of Ngai et al. or Begur et al.

Note, for example, that claims 2 and 10 both refer to a programmable ability to provide operation of channel buffers in a block access mode or in a FIFO access mode. It is clear that Earnest discloses operation only in the FIFO mode. Both of these claims were further clarified to recite, as in claim 2, that the control unit is programmable for operating individual ones of channel buffers in "one of a block access mode and in a first in/first out (FIFO) access mode of operation".

It is noted that in rejecting claims 2 and 10, as well as 15-19, over Earnest in view of Ngai et al., the Examiner refers to col. 7, lines 27-35, of the newly cited Ngai et al. for teaching a memory having a portion that operates in a block access mode (RAM mode) and a section that operates in a FIFO mode (see also Fig. 5 of Ngai et al.)

However, and as was argued above, there is clearly no suggestion in Earnest to use a single dual-ported memory in place of the separate and distinct transmit and receive FIFO memories 16 and 18 and, **in fact, Earnest can actually be read so as to teach away from the use of a single dual ported memory**. This being the case then, **there is clearly no suggestion to substitute the memory cell array 100 of Ngai et al. for the separate and distinct transmit and receive FIFO memories 16 and 18 of Earnest**, and it is respectfully submitted that the Examiner's attempt to do amounts to an impermissible hindsight reconstruction of the prior art devices based on the teachings of the Applicants.

The previously added claim 15 states that a programmable buffer circuit has a control unit programmable by a data processor for specifying:

> "for individual ones of buffers both buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, where said

> control unit is programmable for operating individual ones of said buffers in one of a block access mode of operation and in a first in/first out (FIFO) access mode of operation."

For at least the reasons argued above, claims 15 and 16 are clearly patentable over Earnest in view of Ngai et al.

Claim 17 recites in part that a programmable buffer circuit has a control unit programmable by a data processor for specifying:

> "a control unit programmable by said data processor for specifying individual ones of buffer locations and buffer sizes within said dual port memory for individual ones of said channel interfaces, where there are four transmit registers allocated for each channel interface designated as BaseReg0, BaseReg1, SizeReg0 and SizeReg1 and four receive registers also designated as BaseReg0, BaseReg1, SizeReg0 and SizeReg1, said control unit being responsive to operating in a Block Mode to provide two independent buffers Buffer0 and Buffer1, where BaseReg0 stores the starting address of Buffer0, SizeReg0 specifies the size of Buffer0, BaseReg1 stores the starting address of Buffer1, and SizeReg1 specifies the size of Buffer1 size, said control unit being further responsive to operating in a FIFO Mode to provide one buffer, where BaseReg0 stores the start address of the single buffer, and SizeReg0 specifies the size of the single buffer."

Dependent claim 18 further specifies the operation in the FIFO Mode where the "register BaseReg1 functions as a Low Threshold Register and said register SizeReg1 functions as a High Threshold Register."

Claims 17 and 18 are also clearly patentable over Earnest in view of Ngai et al., first for the reason that there is no express motivation or suggestion to substitute the memory array 100 of Ngai et al. for the FIFOs 16 and 18 of Earnest, as was argued above, and further for the reasons that not all of the specific details of the circuit construction recited in claims 17 and 18, as it pertains to the claimed "dual port memory", is suggested or disclosed by either of Earnest or Ngai et al.

Claim 19 recites in part that a programmable buffer circuit has a control unit programmable by

a data processor, where the control unit is operable to:

> "set up and operate a first portion of said dual port memory in a block mode of operation having a transmit buffer and a receive buffer, and to also operate a second portion of the dual port memory in a FIFO mode of operation having a single buffer."

Dependent claim 20 then further modifies claim 19 by stating that the "first portion of said dual port memory is coupled to a data packet channel interface, and where said second portion of said dual port memory is coupled to an audio CODEC".

For the reasons argued above, claim 19 is patentable over Earnest in view of Ngai et al., and the addition of Begur et al. to this proposed combination of references does not render claim 20 unpatentable.

Claims 1-20 are thus believed to be clearly patentable over Earnest, either alone or in combination with Ngai et al. and/or Begur et al., and the Examiner is respectfully requested to reconsider and remove the final rejections in view of the claims as presented for examination. A favorable reconsideration that results in the allowance of all of the pending claims 1-20 is respectfully requested.

Respectfully submitted:

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